Workshop on layout extraction – Prague, June 2025

Schedule	Day 1 – Mon 9 Jun Inductance, modelling, verification	Day 2 – Tue 10 Jun Resistance, capacitance, dense magnetic coupling	Day 3 – Wed 11 Jun Electrical simulation, LVS and compact models	Day 4 – Thu 12 Jun Flux trapping and moat analysis, frequency response	Day 5 – Fri 13 Jun Advanced analogue circuits, packaging, future
08h00 – 08h30	On-site sign-in and welcome ***C Fourie, M Janosek***				
08h30 – 09h30	**D1S1** InductEx installation, licence key issue and startup ***SM Team***	**D2S1** Resistance, capacitance extraction, characteristic impedance, coupling, magnetic field visualisation ***C Fourie***	**D3S1** JoSIM Pro introduction, working with phase, noise ***J Delport***	**D4S1** Flux trapping analysis in SFQ, AQFP layouts and compact models ***L Johnston***	**D5S1** SQUID magnetometer, gradiometer analysis: effective area, field/flux sensitivity ***T Hall***
09h30 – 10h30	**D1S2** InductEx introduction, layer definition file setup for fab process ***C Fourie***	**D2E2** Add resistance to SFQ layouts and extract example capacitances ***C Fourie***	**D3E2** Model example circuits with JoSIM Pro ***J Delport***	**D4S2** Gibbs energy calculation of trapped flux; critical fields ***K Jackman***	**D5E2** Do exercises on SQUID and gradiometer analysis ***T Hall***
10h30 – 11h00	Break	Break	Break	Break	Break
11h00 – 12h00	**D1S3** Inductance Extraction: basic structures, mastering modelling parameters ***T Hall***	**D2S3** CheckNet validation of coupling between inductors ***K Jackman***	**D3S3** InductEx-LVS: LVS of SFQ, AQFP and chip-level layouts ***K Jackman***	**D4S3** Optimal moat design and analysis ***K Jackman***	**D5S3** Advanced examples – Package modelling, bond wires, bumps, flip-chip and off-chip structures, full SQIF. ***C Fourie***
12h00 – 13h00	**D1E4** Model basic processes and extract inductance of example structures. ***T Hall***	**D2E4** Densely coupled AQFP layouts, loops for superconducting qubits ***C Fourie***	**D3S4** Compact model extraction of SFQ, AQFP and SQIF layouts ***K Jackman***	**D4E4** Do flux trapping exercises, analyse moats, energy and operating limits from layout ***L Johnston***	**D5S4** Upcoming feature showcase. ***C Fourie***
13h00 – 15h00	LUNCH	LUNCH	LUNCH	LUNCH	LUNCH
15h00 – 16h00	**D1S5** Inductance extraction: Basic SFQ layouts, result verification, model inspection, current density plot ***C Fourie***	**D2E5** Do CheckNet examples and model AQFP layouts for extraction ***L Johnston***	**D3E5** Attendee exercises, submitted examples ***SM Team***	**D4S5** S-parameters and filter, resonator frequency analysis ***K Jackman***	**D5E5** Attendee exercises, submitted examples ***SM Team***
16h00 – 17h00	**D1E6** Process example layouts to find inductance ***C Fourie***	**D2P6** Optional attendee poster presentations ***L Johnston***	**D3E6** Attendee exercises, submitted examples ***SM Team***	**D4E6** Frequency analysis examples ***K Jackman***	**D5E6** Attendee exercises, submitted examples ***SM Team***